What is claimed is:

1. A method for manufacturing a semiconductor apparatus comprising the steps of:

forming a semiconductor over a substrate;

forming a mask comprising a resist over the semiconductor to overlap with a portion of the semiconductor; and

adding an impurity element to the semiconductor in accordance with the mask by a doping method;

wherein an area of the mask is smaller than that of a mask which has an opening only in an impurity element doped region and in an adjusting margin over the semiconductor.

2. A method for manufacturing a semiconductor apparatus comprising the steps of:

forming a semiconductor over a substrate;

forming a mask comprising a resist over the semiconductor to overlap with a portion of the semiconductor; and

adding an impurity element to the semiconductor in accordance with the mask by a doping method with acceleration voltage of at least 80kV;

wherein an area of the mask is at most 15% of an area of the substrate.

3. A method for manufacturing a semiconductor apparatus comprising the steps of:

forming a semiconductor over a substrate;

forming a mask comprising a resist over the semiconductor to overlap with a portion of the semiconductor and heating the resulted mask; and

adding an impurity element to the semiconductor in accordance with the mask by a doping method;

wherein an area of the mask is smaller than that of a mask which has an opening only in an impurity element doped region and in an adjusting margin over the semiconductor.

4. A method for manufacturing a semiconductor apparatus comprising the steps of:

forming a semiconductor over a substrate;

forming a mask comprising a resist over the semiconductor to overlap with a portion of the semiconductor and heating the resulted mask; and

adding an impurity element to the semiconductor in accordance with the mask by a doping method with acceleration voltage of at least 80kV;

wherein an area of the mask is at most 35% of an area of the substrate.

5. A method for manufacturing a semiconductor apparatus comprising the steps of:

forming a semiconductor over a substrate;

forming a gate electrode over the semiconductor via an insulating film;

forming a first mask comprising a resist in a position to overlap with a portion of the semiconductor;

adding an n-type impurity element to the semiconductor in accordance with the

mask by a doping method with acceleration voltage of at least 60kV;

removing the first mask;

forming a second mask comprising a resist in a position to overlap with a portion of the semiconductor; and

adding a p-type impurity element to the semiconductor in accordance with the mask by a doping method with acceleration voltage of at least 80kV;

wherein an area of the first mask is at most 20% of an area of the substrate, and an area of the second mask is at most 15% of an area of the substrate.

6. A method for manufacturing a semiconductor apparatus comprising the steps of:

forming a semiconductor over a substrate;

forming a gate electrode over the semiconductor via an insulating film;

forming a first mask comprising a resist in a position to overlap with a portion of the semiconductor and heating the resulted first mask;

adding an n-type impurity element to the semiconductor in accordance with the mask by a doping method with acceleration voltage of at least 60kV;

removing the first mask;

forming a second mask comprising a resist in a position to overlap with a portion of the semiconductor and heating the resulted second mask; and

adding a p-type impurity element to the semiconductor in accordance with the mask by a doping method with acceleration voltage of at least 80kV;

wherein an area of the first mask is at most 40% of an area of the substrate, and an area of the second mask is at most 35% of an area of the substrate.

7. A method for manufacturing a semiconductor apparatus comprising the steps of:

forming a semiconductor over a substrate;

forming a gate electrode over the semiconductor via an insulating film;

forming a first mask comprising a resist in a position to overlap with a portion of the semiconductor;

adding an n-type impurity element to the semiconductor in accordance with the mask by a doping method with current density of at least $15\mu A/cm^2$ and with acceleration voltage of at least 60kV;

removing the first mask;

forming a second mask comprising a resist in a position to overlap with a portion of the semiconductor; and

adding a p-type impurity element to the semiconductor in accordance with the mask by a doping method with current density of at least $15\mu A/cm^2$ and with acceleration voltage of at least 80kV;

wherein an area of the first mask is at most 20% of an area of the substrate, and an area of the second mask is at most 15% of an area of the substrate.

8. A method for manufacturing a semiconductor apparatus comprising the steps of:

forming a semiconductor over a substrate;

forming a gate electrode over the semiconductor via an insulating film;

forming a first mask comprising a resist in a position to overlap with a portion

of the semiconductor and heating the resulted first mask;

adding an n-type impurity element to the semiconductor in accordance with the mask by a doping method with current density of at least 15μA/cm^2 and with acceleration voltage of at least 60kV;

removing the first mask;

forming a second mask comprising a resist in a position to overlap with a portion of the semiconductor and heating the resulted second mask; and

adding a p-type impurity element to the semiconductor in accordance with the mask by a doping method with current density of at least 15μA/cm^2 and with acceleration voltage of at least 80kV;

wherein an area of the first mask is at most 40% of an area of the substrate, and an area of the second mask is at most 35% of an area of the substrate.

9. A semiconductor apparatus including a plurality of an n-channel TFT or a p-channel TFT over a substrate, comprising:

an island like semiconductor including an n-type impurity region and an island like semiconductor including a p-type impurity region over the substrate;

an insulating film formed over the substrate to cover the island like semiconductor including the n-type impurity region and the island like semiconductor including the p-type impurity region; and

a gate electrode formed to overlap a portion of the island like semiconductor including the n-type impurity region and a portion of the island like semiconductor including the p-type impurity region via the insulating film;

wherein an impurity concentration of the insulating film is lower than that of

another region in a position which is overlapping with the n-type impurity region.

10. A display device including a plurality of pixel portions, and a plurality of an n-channel TFT or a p-channel TFT over a substrate, comprising:

an island like semiconductor including an n-type impurity region and an island like semiconductor including a p-type impurity region over the substrate;

an insulating film formed over the substrate to cover the island like semiconductor including the n-type impurity region and the island like semiconductor including the p-type impurity region; and

a gate electrode formed to overlap a portion of the island like semiconductor including the n-type impurity region and a portion of the island like semiconductor including the p-type impurity region via the insulating film;

wherein a part of the pixel portion contains a n-type impurity element and a p-type impurity element.

11. A display device according to claim 10, wherein a ratio of the part of the pixel portion containing impurity element to the pixel portion is no less than 80 %.

12. A method for manufacturing a semiconductor apparatus according to claim 1, wherein the semiconductor apparatus is a display device.

13. A method for manufacturing a semiconductor apparatus according to claim 2, wherein the semiconductor apparatus is a display device.

14. A method for manufacturing a semiconductor apparatus according to claim 3, wherein the semiconductor apparatus is a display device.

15. A method for manufacturing a semiconductor apparatus according to claim 4, wherein the semiconductor apparatus is a display device.

16. A method for manufacturing a semiconductor apparatus according to claim 5, wherein the semiconductor apparatus is a display device.

17. A method for manufacturing a semiconductor apparatus according to claim 6, wherein the semiconductor apparatus is a display device.

18. A method for manufacturing a semiconductor apparatus according to claim 7, wherein the semiconductor apparatus is a display device.

19. A method for manufacturing a semiconductor apparatus according to claim 8, wherein the semiconductor apparatus is a display device.

20. A method for manufacturing a semiconductor apparatus according to claim 12, wherein a area of the substrate is no less than 1 square meter.

21. A method for manufacturing a semiconductor apparatus according to claim 13, wherein a area of the substrate is no less than 1 square meter.

22. A method for manufacturing a semiconductor apparatus according to claim 14, wherein a area of the substrate is no less than 1 square meter.

23. A method for manufacturing a semiconductor apparatus according to claim 15, wherein a area of the substrate is no less than 1 square meter.

24. A method for manufacturing a semiconductor apparatus according to claim 16, wherein a area of the substrate is no less than 1 square meter.

25. A method for manufacturing a semiconductor apparatus according to claim 17, wherein a area of the substrate is no less than 1 square meter.

26. A method for manufacturing a semiconductor apparatus according to claim 18, wherein a area of the substrate is no less than 1 square meter.

27. A method for manufacturing a semiconductor apparatus according to claim 19, wherein a area of the substrate is no less than 1 square meter.